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UTILIZATION OF AN ELECTRONIC CIRCUIT SIMULATOR IN CMOS LATCH-UP STUDIES

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ABSTRACT

The 2-D device simulator presented in this work allows the investigation of the effect of ionizing radiation dose rate on the performance of CMOS circuits. The simulator is composed of two parts, a diffusion current module and a lumped-element module.

The first module solves the current transport equations with the aid of the HSPICE code. The lumped-element module then simulates the electrical characteristics of the parasitic pnpn structure (present in CMOS circuits) using the results from the first module as input parameters. The model was applied to study the latch-up vulnerability of a CMOS inverter as a function of circuit layout and distribution of substrate contacts. Results of radiation hardening efforts are presented.

RESUME

Le simulateur de composants à deux dimensions présenté dans ce rapport permet l'investigation des effects du taux d'irradiation sur les performances des circuits CMOS. Le simulateur se compose de deux parties, le module de courant de diffusion et le module d'éléments regroupés.

Le premier module solutionne les équations du courant de diffusion à l'aide du logiciel HSPICE. Ensuite, le module d'éléments regroupés simule les caractéristiques électriques de la structure PNPN parasite (présente dans les circuits CMOS) en utilisant les résultats obtenus à partir du premier module comme paramètres d'entrée. Le modèle a été utilisé pour étudier la vulnérabilité de verrouillage d'un inverseur CMOS en fonction de l'agencement et de la distribution des contacts du substrat. Les résultats des tentatives d'insensibilisation aux radiations sont présentés.

EXECUTIVE SUMMARY

The performance of CMOS-based technology VLSI is known to be vulnerable to latch-up, a state of self-sustaining low impedance, during which large current flow takes place within the substrate of the circuit. Latch-up in CMOS circuits can occur through an overvoltage pulse or via ionizing radiation and will lead to signal upset or even circuit burnout.

The work presented here is related to radiation-induced latch-up simulations in CMOS circuits using a computer model developed at DREO. The advantage of using a computer model for an application such as this one is that the changes to circuit layout and parameters are easily implemented. This is very useful when evaluating the radiation hardness of a circuit or designing a new one, as the investigator may have to go through several layout iterations before reaching the optimum configuration.

Results of simulations, using a CMOS inverter, conclusively indicated the importance of circuit layout and distribution of substrate contacts on the circuit vulnerability to ionizing radiation effects. Radiation hardening efforts that had been carried out on a standard reference model of a CMOS inverter, have resulted in a substantial increase of the latch-up threshold dose rate for some of the circuit layouts.

In addition to latch-up vulnerability evaluation of CMOS circuits, the model can also be used in upset-sensitive area mapping and device optimization.

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1.0 Introduction

Radiation effects on the performance of electronic devices and circuits are becoming increasingly more important as the devices are being scaled down and new technologies are being introduced. As the vulnerability of the equipment to radiation stress increases with decreasing feature size of components and circuits, ionizing radiation may create serious reliability problems in the future military/aerospace systems. Radiation vulnerability studies will have to be included into the developmental stage of new device and circuit fabrications.

A specific type of circuits whose functionality is vulnerable to radiation effects are the CMOS VLSI (Very Large Scale Integration) circuits. In the radiation environment, the CMOS VLSI systems can enter into a state of self-sustaining low impedance (latch-up) during which large current flow takes place through the substrate of the circuit. Latch-up usually results in a circuit function upset or even a circuit burnout.

The latch-up vulnerability of CMOS VLSI circuits comes from the inherent pnpn structure forming a pair of bipolar parasitic transistors. Figure 1a is a cross-sectional view of a CMOS inverter showing the parasitic transistor pair and the major currents involved in the latch-up process. Latch-up studies in CMOS VLSI have been largely carried out utilizing a two transistor lumped element model (with some minor variations[1-3]) such as the one shown in figure 1b. The model shows the regenerative coupling between the pnp and npn transistors and the shunting resistors that maintain the bias on the emitters of the two devices during latch-up. The shunting resistance R_{sub} in the model is the substrate resistance between the Vdd N+ contact and the P+ diffusion well (the emitter of the parasitic pnp transistor)

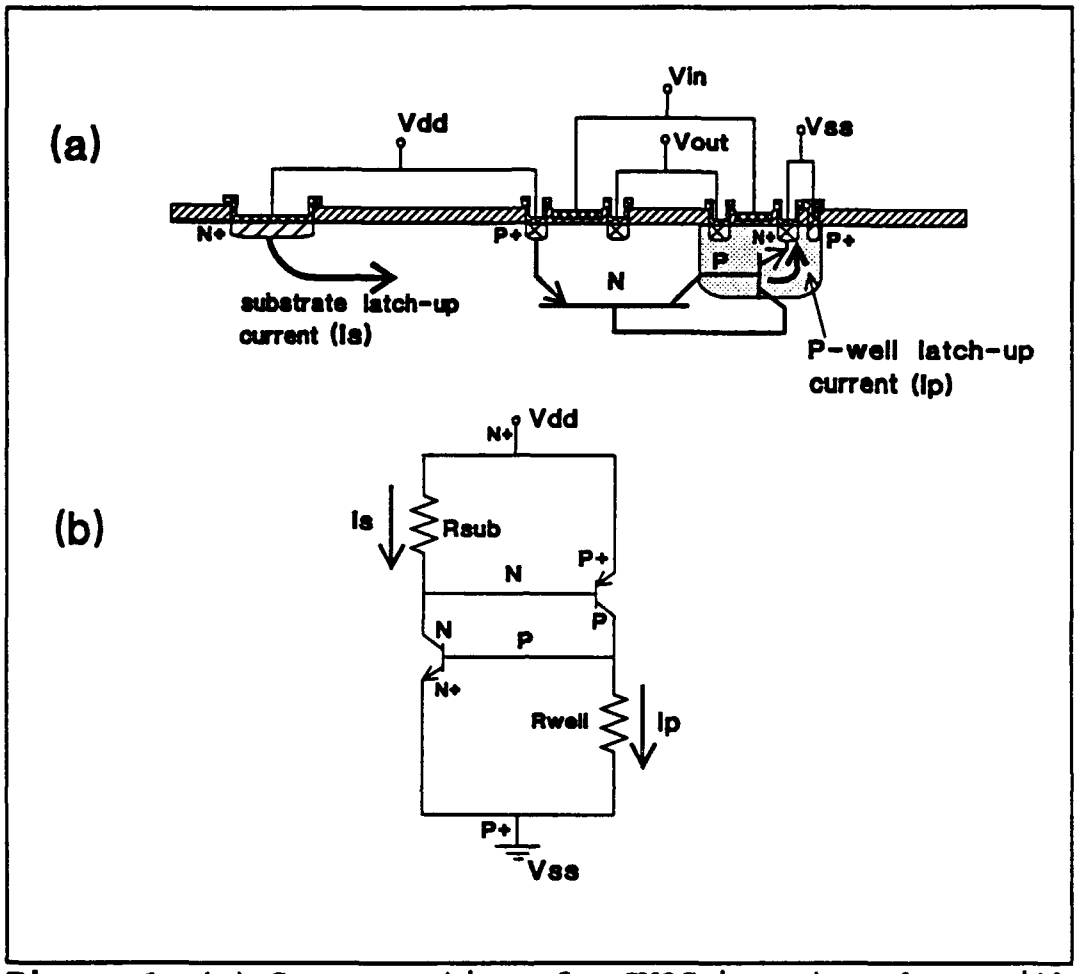

Figure 1: (a) Cross-section of a CMOS inverter shown with the parasitic pnpn structure and associated latch-up currents
(b) Basic equivalent two-transistor model for latch-up study

and R_{well} is the P-well resistance between the Vss P+ contact and the N+ well.

Results from previous studies point to two stages that are associated with latch-ups, namely the triggering stage and the holding stage[4]. During the normal CMOS operation, both sides of the P+/N-substrate and the N+/P-well junctions are at the same potential while the

P-well/N-substrate junctions are reverse biased by V_{dd} volts. The triggering mechanism will differ with the nature of the stimulus. It can occur either through the voltage drop across R_{sub} (overvoltage stress) or photocurrent accumulation at the junctions (radiation stress). A latch-up holding stage will occur only if the voltage drops in the substrate and the P-well are able to maintain the two transistors in the active mode.

Utilization of a computer model for latch-up prediction in CMOS circuits is a valuable tool, either when used in evaluating the latch-up vulnerability of an existing circuit or as a means of providing guidance for new circuits design. The aim of this work is to present a 2-D model that can be used for such a purpose. The work presented illustrates the application of an electronic circuit simulator, namely the HSPICE code, as means of carrying-out equilibrium finite element analysis of potential, current and current carrier distribution in CMOS circuits prior to and during latch-up. The model presented consists of two modules, namely the "diffusion current module" and the "lumped-element module". In the diffusion module, the transport equations for the current carriers are solved and the results are then subsequently used in the lumped-element module. In the lumped-element module, the devices participating in the latch-up, namely the parasitic bipolar junction transistors, are entered into the model in their equivalent circuit forms. Additional model features are also included to enable the initiation of the transistor action and hence the ability of the circuit to latch-up.

The model has been subjected to common CMOS circuit radiation hardening techniques. The results show that the model responds to proven hardening techniques in agreement with the observed responses of real integrated circuits.

2. The Diffusion Model

2.1 Minor Carriers Transport

2.1.1 Approach Formulation to Modelling

Transport phenomena in a semiconductor medium can be described by three equations, namely the Poisson equation

$$\nabla\cdot(\epsilon\nabla\Psi) = -q(p-n+N_D^+-N_A^-) \tag{2.1}$$

and continuity equations for holes and electrons given by

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla\cdot J_p - R \tag{2.2}$$

and

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla\cdot J_n - R \tag{2.3}$$

The currents in (2.2) and (2.3) have both the diffusion and the drift components given by

$$J_p = -q\mu_p p\nabla\Psi - qD_p\nabla p \tag{2.4}$$

and

$$J_n = -q\mu_n n\nabla\Psi + qD\nabla n \tag{2.5}$$

where Ψ is the electric potential function, q is the magnitude of the electronic charge, ϵ is dielectric permittivity, N_D^+ and N_A^+ are the concentrations of ionized donors and acceptors and p and n are current carriers. In the continuity equations (2.2) and (2.3), R is the carrier's recombination term.

Computer codes such as PISCES[5] or SITAR[1] for example, solve the above equations using Gummel's iteration method. First the Poisson equation is solved with assumed quasi-Fermi potentials for holes and electrons. The calculated

electric potentials Ψ from the first step are then used in solving the continuity equations. The new carrier densities are then substituted back into Poisson equation and the steps are repeated until convergence is reached.

An alternative approach, adopted in this work, is based on total current conservation[2], specifically, the divergence of currents within any volume of a device is zero for a given boundary condition. Taking the time derivative of the Poisson equation (2.1) and then substituting equations (2.2) and (2.3) into R.H.S. of (2.1) will lead to Kirchhoff's current relation at a particular point x,y

$$\nabla \cdot J_t = 0 \tag{2.6}$$

with the total current density J_t given by

$$J_t = J_p + J_n + \epsilon \frac{\partial}{\partial t} E \tag{2.7}$$

where the last term in (2.7) is the displacement current. Equations (2.6) and (2.7) can then be used as the starting point in defining the basic equations for a particular type of transport application.

2.1.2 Diffusion Field - Resistive Field Analog

A 2-D equilibrium situation concerning motion of minority carriers in the absence of an electric field reduces (2.6) and (2.7) to a steady state diffusion equation. In rectangular coordinates such an equation in the extrinsic semiconductor is given by

$$D\nabla^2 P(x,y) - \frac{P(x,y)}{\tau} = 0 \tag{2.8}$$

where P(x,y) is the excess of minority carriers above the thermal equilibrium concentration, D is the diffusion coefficient for a particular carrier type and τ is the doping

dependent average lifetime of minority current carriers in the extrinsic semiconductor.

For simple boundary conditions, the exact solution to a partial differential equation (2.1) can be found, however, often it impossible to obtain an exact analytic function satisfying both the equation and the imposed boundary conditions. A polynomial solution may satisfy both the equation and the boundary conditions, but its physical meaning is difficult to interpret. Transformation of the continuous equation into a finite difference equation is frequently used to solve the problem at hand.

To convert from continuous to a discrete spatial domain, the following two-grid mesh definition is introduced

$$x=>x_i;\quad i=1,.....m;\quad x_{i+1}-x_i=\frac{h_i+h_{i+1}}{2};\quad P(x,y)=>P(x_i,y_j) \qquad (2.9)$$

$$y=>y_j;\quad j=1,.....n;\quad y_{j+1}-y_j=\frac{k_j+k_{j+1}}{2} \qquad (2.10)$$

Graphically, this is depicted in figure 2 showing the nonuniform two-grid mesh. The justification for utilizing a two-grid approach will be more obvious later when dealing with the block resistances. It is assumed that the distance between neighbouring nodes is small and that the restrictions imposed by the mean value theorem are met over the i-1 to i+1 interval. Newton's divided difference then can be used in defining the discrete derivatives of P(x,y)[6]. For the grid defined above

$$P[x_{i+1},y_j,x_{i-1},y_j]\equiv\frac{P(x_{i+1},y_j)-P(x_{i-1},y_j)}{\frac{1}{2}h_{i+1}+h_i+\frac{1}{2}h_{i-1}}\approx\frac{\partial P(x,y)\,|x_i,y_j}{\partial x} \qquad (2.11)$$

is the first discrete partial derivative of P(x,y) at the interior point $x=x_i, y=y_j$ of the grid. The derivatives in the y direction are defined analogously.

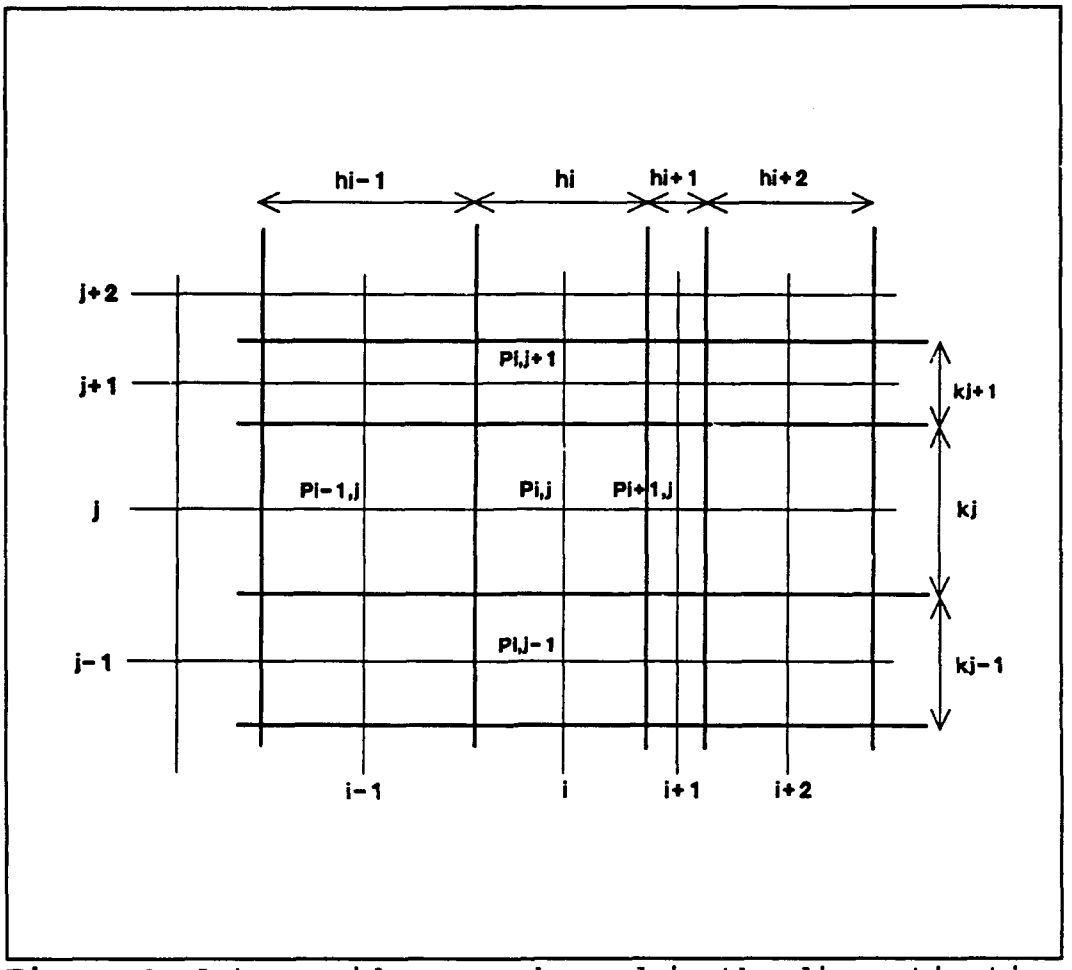

Figure 2: A two-grid approach used in the discretization scheme

Nested utilization of the divided difference yields the second order partial derivatives of P(x,y) at $x=x_i, y=y_j$ [6]

$$\frac{\partial^2 P(x,y)\,|x_i,y_j}{\partial x^2} \approx \frac{1}{h_i}\{P[x_{i+1},x_i,y_j] - P[x_i,x_{i-1},y_j]\} \qquad (2.12)$$

$$\frac{\partial^2 P(x,y)\,|x_i,y_j}{\partial y^2} \approx \frac{1}{k_j}\{P[x_i,y_{j+1},y_j] - P[x_i,y_j,y_{j-1}]\} \qquad (2.13)$$

The partial differential diffusion equation (2.8) can now be replaced by the divided difference equation utilizing the terms from (2.12) and (2.13) which leads to

$$\left[\frac{P(x_{i-1},y_j)-P(x_i,y_j)}{\frac{1}{2}(h_i+h_{i-1})}-\frac{P(x_i,y_j)-P(x_{i+1},y_j)}{\frac{1}{2}(h_i+h_{i+1})}\right]/h_i+$$

$$\left[\frac{P(x_i,y_{j-1})-P(x_i,y_j)}{\frac{1}{2}(k_j+k_{j-1})}-\frac{P(x_i,y_{j+1})-P(x_i,y_j)}{\frac{1}{2}(k_j+k_{j+1})}\right]/k_j+\frac{P(x_i,y_j)}{D\tau}=0 \qquad (2.14)$$

The first two terms in (2.14) represent the divergence of the diffusion current and the last term is due to recombination.

Consider the resistance grid shown in figure 3a with equilibrium currents flowing in each quadrant. Using Kirchhoff's current law, the currents i_1, i_2, i_3 and i_4 flowing into node 0 will be related by the expression

$$\sum_i \frac{V_i-V_0}{R_i}=0; \qquad i=1,..4 \qquad (2.15)$$

Additional currents may added to the original loop such as, for example, a drain current I_d flowing out the central node through a drain resistance R_d as shown in figure 3b. Application of Kirchhoff's current law, will then yield

$$\sum_i \frac{V_i-V_0}{R_i}+\frac{V_0}{R_d}=0; \qquad i=1,..4 \qquad (2.16)$$

A general case is considered in figure 4 which shows a region of a semiconductor subdivided into smaller blocks (heavy lines) having dimensions given by h_i and k_j. The resistance between the two neighbouring nodes in the i and j direction is

$$R_{i,i+1,j}=\frac{\rho 1/2\,(h_i+h_{i+1})}{Tk_j}; \qquad R_{i,j,j+1}=\frac{\rho 1/2\,(k_j+k_{j+1})}{Th_i} \qquad (2.17)$$

where T is the thickness of the block (considered to be constant in a 2-D case) and ρ is doping-dependent specific

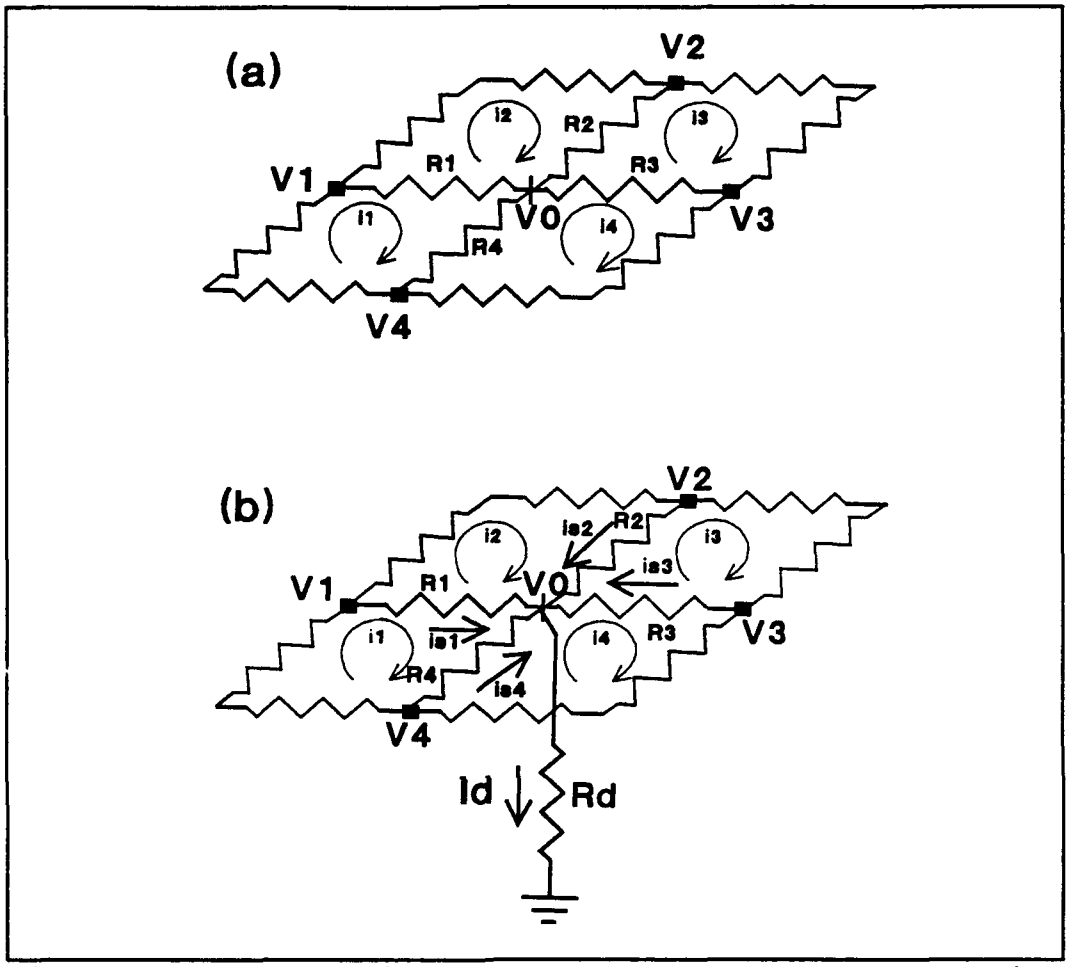

Figure 3: Analog resistance networks approach for solving partial differential equations

resistivity of the semiconductor material. The current conservation applied to a node located inside a semiconductor block gives

$$\frac{Tk_i[V_{i-1,j}-V_{i,j}]}{\rho\frac{1}{2}(h_i+h_{i-1})}+\frac{Tk_i[V_{i,j}-V_{i+1,j}]}{\rho\frac{1}{2}(h_i+h_{i+1})}+\frac{Th_j[V_{i,j-1}-V_{i,j}]}{\rho\frac{1}{2}(k_j+k_{j-1})}+\frac{Th_j[V_{i,j}-V_{i,j+1}]}{\rho\frac{1}{2}(k_j+k_{j+1})}-\frac{V_{i,j}}{Rd_{i,j}}=0 \qquad (2.18)$$

A numerical equivalence between (2.14) and (2.18) can be obtained if (2.14) is multiplied by Th_ik_j/ρ. This permits the distribution of the minority current carriers inside a semiconductor medium to be determined by utilizing a

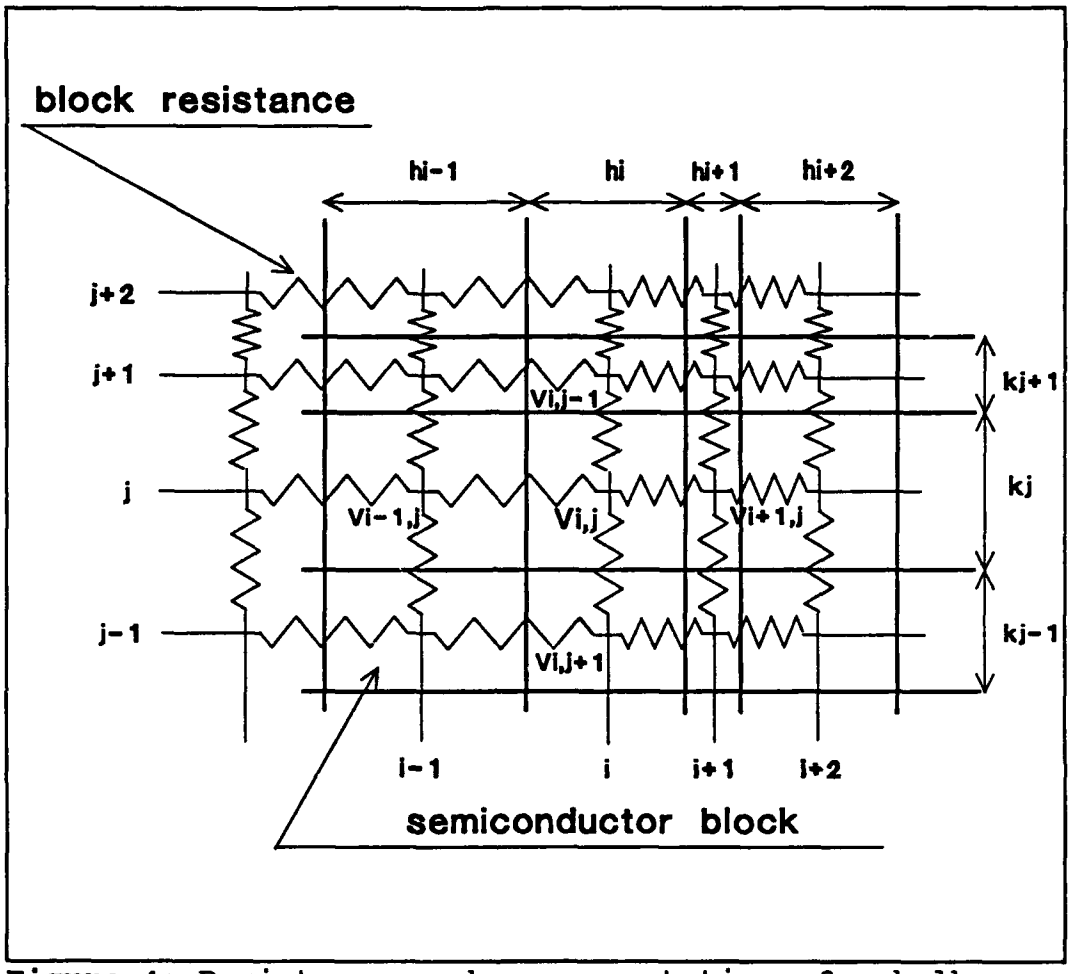

Figure 4: Resistance mesh representation of a bulk semiconductor

resistance grid with appropriate boundary conditions and solving for the node voltages. Such calculations can, as will be indicated, be carried out with an electronic circuit simulator code.

2.2 Diffusion Model of a Simple CMOS Inverter

2.2.1 Substrate Grid

Computation of the diffusion current distribution involved first overlaying the device layout diagram with a coarse rectangular grid. To accommodate the increased geometrical complexity around the diffusion wells,

additional mesh refinements were then made in this region (figure 5). The mesh size selection is affected by the amount of computer memory available and by the cpu time needed to complete the calculations. Additional parameters, such as the number of active and passive devices connected to the grid will further constrain the number of nodes in the mesh, due to increased memory requirements. The above constraints will also affect the accuracy of the results. Reduction in the number of nodes in the grid will increase the residual error inherent in discrete models. Such an error, resulting from the discrepancy between the true value of the function in the continuous domain and the extrapolated value of the function in the discrete domain, will depend on the degree of variation of the function within the sampling interval and the magnitude of the sampling interval.

An estimate of the residual error associated with a node voltage of the model can be performed graphically by determining the asymptote node voltage value $V_{ai,j}$ (an estimate of the continuum) obtained from the plot of $V_{i,j}$ vs number of nodes as shown in figure 6. The deviation of the node voltage from its asymptote value depends on the position of the node on the grid (8 traces in figure 6 represent eight randomly selected points) and on the number of nodes in the grid. For example for a 9 x 3 2-D mesh, the relative residual error can be as high as 30%. By reducing the sampling interval by a factor of to 8, the residual error will reduce to about 3%.

After a grid, as defined by (2.9) and (2.10), was overlaid over the device area of interest, a resistance mesh was generated by interconnecting the nodes of the diffusion grid with resistors having resistances defined by (2.17). Presently, the investigator is not relieved of the burden of designing the grid overlay (carried out by utilizing a CAD software), but the analog resistance mesh generation and placement of appropriate boundary conditions is done automatically by a software written by the author for this purpose. The program called "Discrete Device Generator" (DDG), interconnects the resistors in 2-D or 3-D mesh configuration.

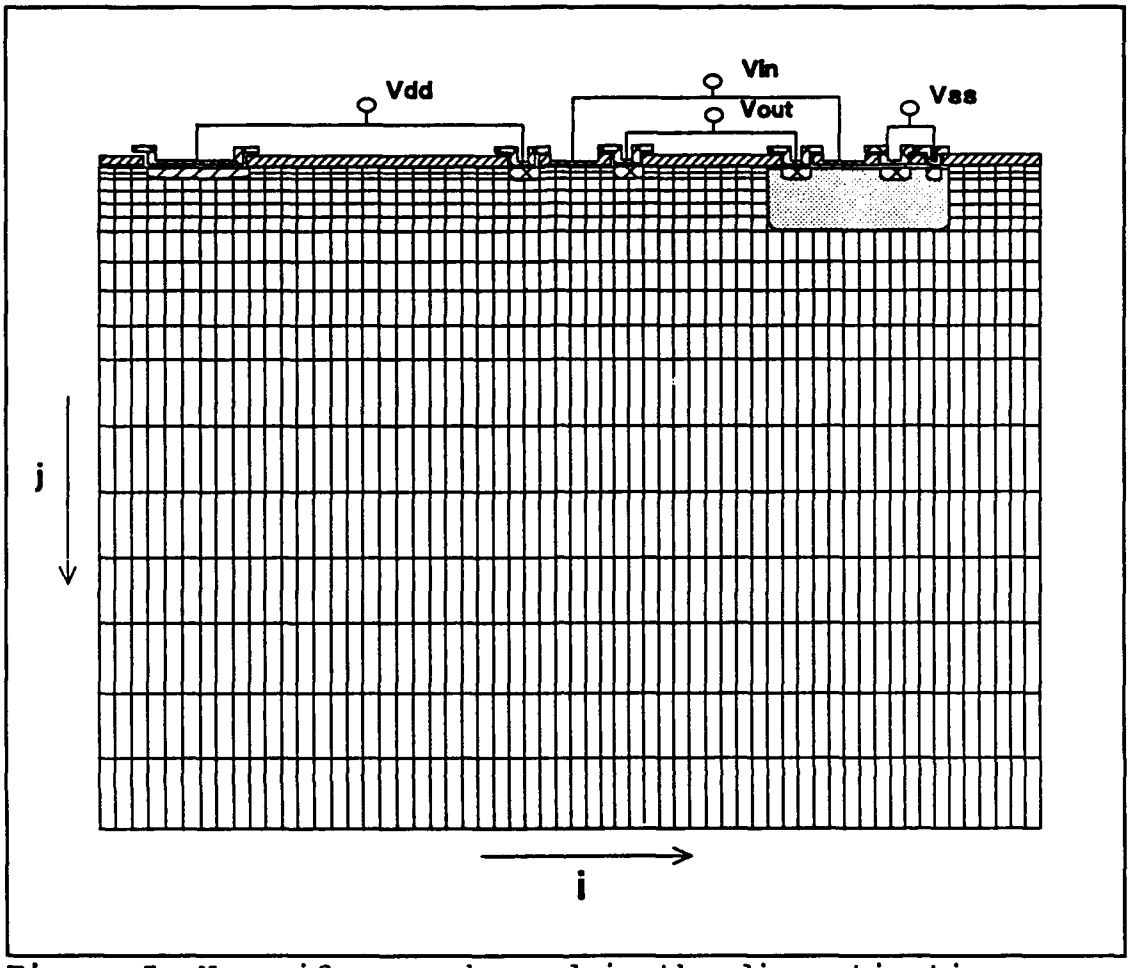

Figure 5: Nonuniform mesh used in the discretization scheme of the CMOS inverter substrate.

For input, the program requires the mesh size (m,n) and locations of the boundaries of diffusion wells. In addition, basic physical and doping parameters of the device are also required as input. The output of DDG forms the main module of the HSPICE input file. Additional data-reduction software has also been written (by the author) for manipulation and display of the HSPICE output files. Figure 7 is the activity flowchart showing the steps involved during the model generation.

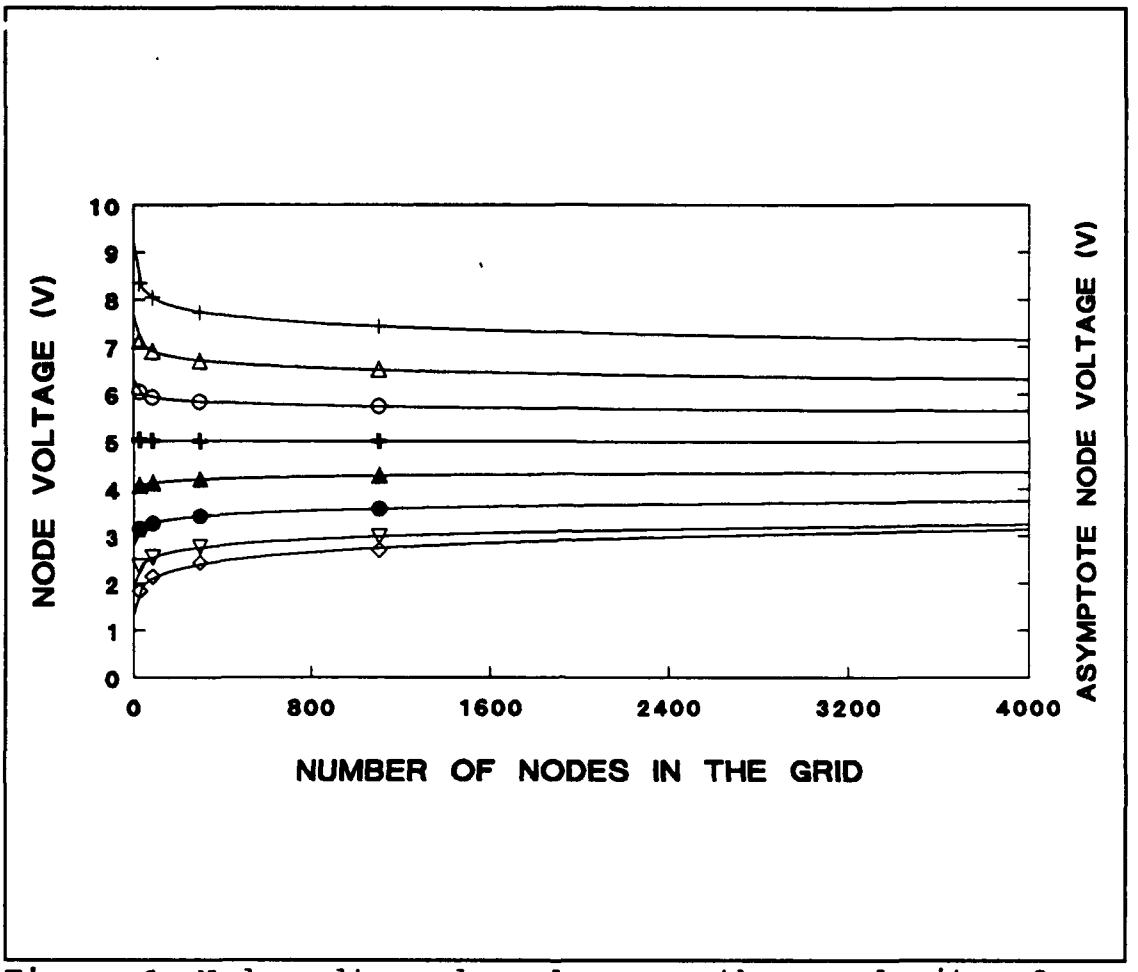

Figure 6: Node voltage dependence on the complexity of the grid. The voltages will asymptotically approach limiting values as the number of nodes in the grid increase.

2.2.2 Emitter-Base Boundary

In the diffusion model, the emitter/base boundaries have been implemented as regions where the concentration of minority carriers is constant. The concentration of mobile carriers at these boundary nodes is given by the Boltzman-Shockley relation

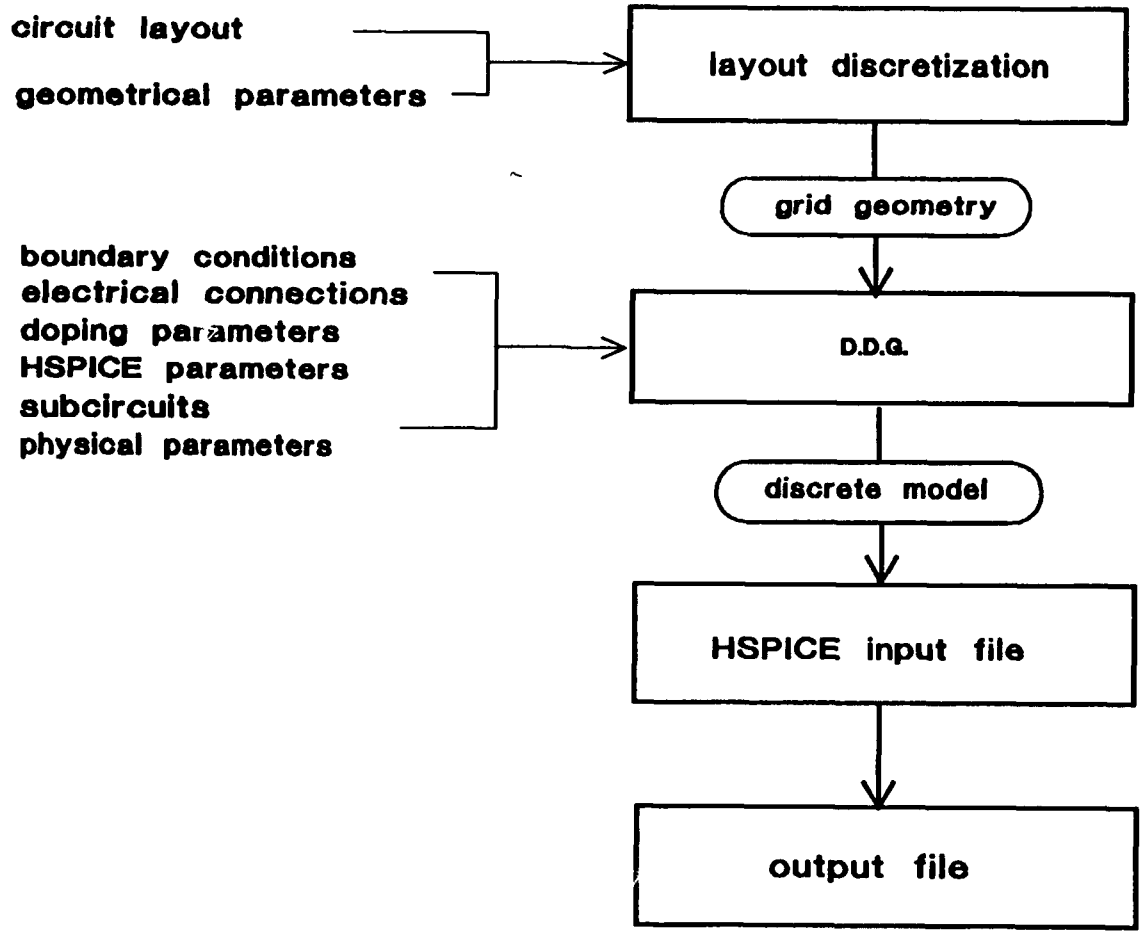

Figure 7: Sequence of steps involved during the model generation.

$$P_0(x_i,y_j) = p_0(x_i,y_j)\,(\exp\frac{qV_d}{kT}-1) \qquad (2.19)$$

with $p_0(x_i,y_j)$ as the concentration of carriers given by Boltzmann statistics and $P_0(x_i,y_j)$ as the excess concentration of carriers under the forward bias condition ($V_d > 0$). A constant concentration of minority carriers at these nodes allows for implementation of a simple Dirichlet[6] boundary at this region of the mesh. This is done by utilization of independent voltage sources connected between the ground and the nodes surrounding the emitter as shown in figure 8a.

2.2.3 Depletion Region

A depletion region on the diffusion grid acts as a strong drain of mobile current carriers due to the "vacuum" action of the electric field set up by the contact potential. The following abrupt junction definition[7] has been made in order to implement the depletion regions on the electrical grid:

i) concentration of current carriers inside the depletion region is zero

ii) the concentration current carriers changes abruptly to a thermal equilibrium level outside the depletion region boundary.

With no free current carriers present, the depletion regions were implemented on the electrical grid by connecting the grid nodes at these regions to the ground[8] as depicted in Figure 8c.

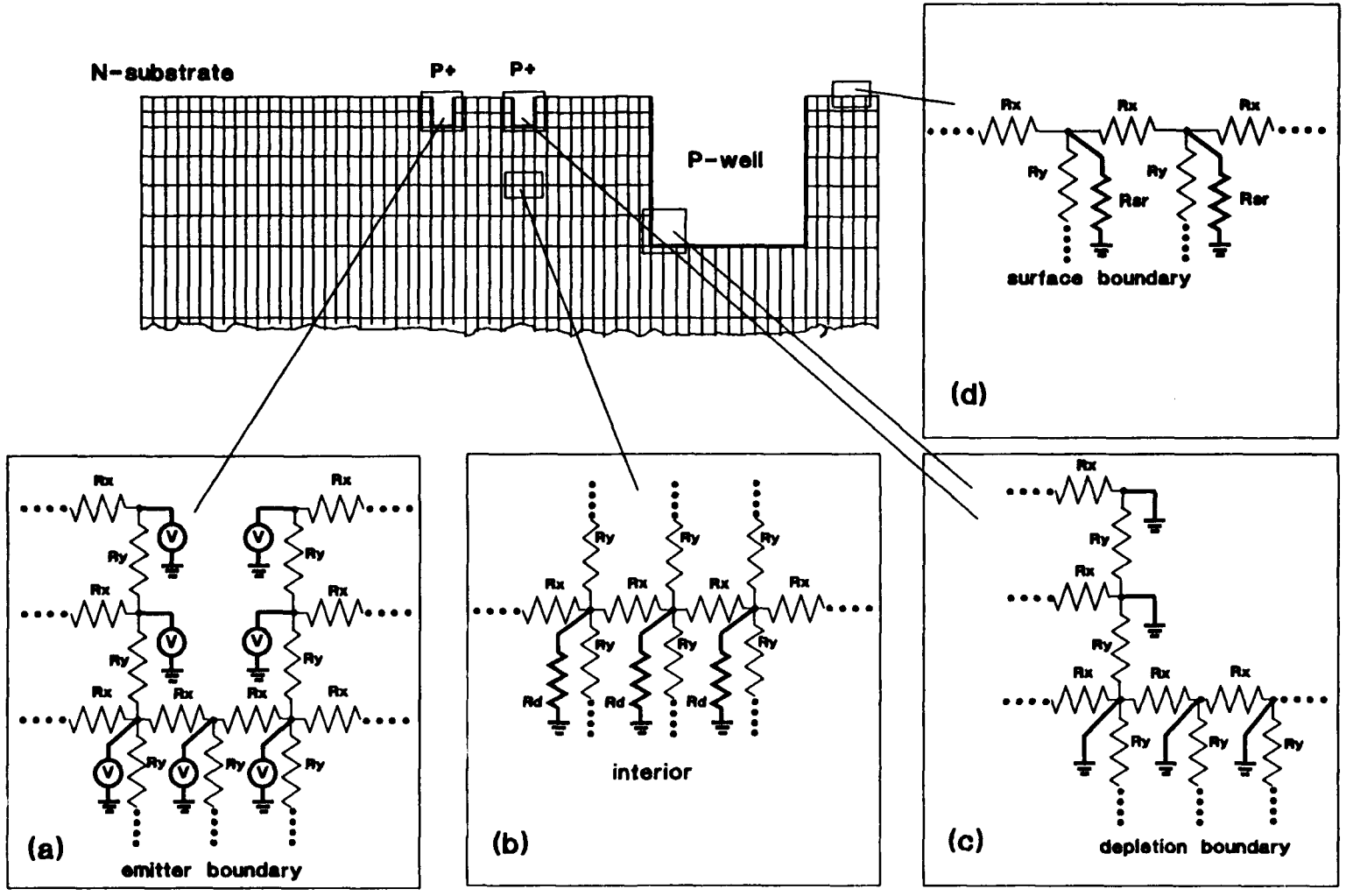

Figure 8: The electrical analog of the diffusion current model for a CMOS inverter.

2.2.4 Surface Boundary

The fabrication process makes the surface of a semiconductor a site for removal of minority current carriers. Removal of carriers at the surface generates a gradient in minority carriers concentration resulting in a net diffusion current flowing normal toward the surface. For example, the recombination current at a specific surface node x_1, y_j on the diffusion grid is[8]

$$I_{surface} = qP(x_1, y_j)\, v_s \tag{2.20}$$

where v_s is the surface recombination velocity. The normal diffusion current due to a such recombination is

$$I_{\perp} = qD \frac{P(x_2, y_j) - P(x_1, y_j)}{\frac{1}{2}(h_2 + h_1)} \tag{2.21}$$

Under equilibrium condition, the two currents are balanced giving

$$\frac{P(x_1, y_j) - P(x_2, y_j)}{\frac{P(x_1, y_j)}{2}(h_1 + h_2)} = -\frac{v_s}{D} \tag{2.22}$$

On the electrical mesh, the surface recombination resistance $Rsr_{1,j}$ connected to the ground (figure 8d, no subscripts shown) is the electrical analog to surface recombination. The current I that flows from a particular surface node 1,j through the surface recombination resistance $Rsr_{1,j}$ into the ground is simply given by

$$\frac{V_{1,j}}{Rsr_{1,j}} = I \tag{2.23}$$

Current conservation requires an equivalent normal current component to flow into the 1,j node according to

$$\frac{V_{2,j}-V_{1,j}}{\frac{\rho}{2}\frac{(h_1+h_2)}{Tk_j}} = I \qquad (2.24)$$

Equating (2.23) with (2.24) will result in

$$\frac{V_{2,j}-V_{1,j}}{\frac{V_{1,j}}{2}(h_1+h_2)} = \frac{\rho}{Tk_j Rsr_{1,j}} \qquad (2.25)$$

A term by term comparison of (2.25) with (2.22) gives the expression for the surface recombination resistance $Rsr_{1,j}$ as

$$Rsr_{1,j} = \frac{\rho D}{Tk_j v_s} \qquad (2.26)$$

2.3.6 Bulk Recombination

At the diffusion mesh nodes, the mobile current carriers are subjects to excessive recombination when their concentration is above the thermal equilibrium concentration ($np > n_i^2$). The diffusion model supports simple recombination given by

$$Rd_{i,j} = \frac{P(x_i, y_j)}{\tau} \qquad (2.27)$$

The equivalent electrical analog[9] to recombination is shown in figure 8b (drain resistors shown without subscripts). From the arguments developed in Section 2., the magnitudes of individual drain resistors $Rd_{i,j}$ can be obtained by equating the recombination expression in (2.14) with the drain expression in (2.18) giving

$$\frac{P(x_i, y_j)\, Th_i k_j}{D\rho\tau} = \frac{V_{i,j}}{Rd_{i,j}} \qquad (2.28)$$

with $Rd_{i,j} = D\tau\rho/Th_i k_j$. The current flow through the drain resistor $Rd_{i,j}$ will reduce the voltage at the node x_i, y_j by the amount proportional to the reduction of minority current carriers concentration caused by the recombination loss.

3. Diffusion Current Distribution - Model Application

The diffusion model was used to create a steady state minority current carrier distribution map inside the substrate and the P-well of a CMOS inverter with active parasitic pnp and npn transistors. The information available from such a mapping was then used to determine the current-gain parameters for the two transistors. The geometrical parameters (Table 1) that were utilized in this basic reference model of the inverter, have been adopted from the associated CMOS input/buffer circuitry of the Siliconix DG 515 D/A converter[10]. The doping parameters, also from the same reference, $N_d = 1 \times 10^{15}$ cm^{-3} (substrate) and $N_a = 2 \times 10^{16}$ cm^{-3} (P-well) were used in calculating the specific resistances of the semiconductor regions that were modelled. Table 2 provides a list of the nodal separations inside the substrate resistance grid and Table 3 lists additional input parameters that were also used in the model. A regular rectangular grid was used in the P-well region with nodal separations of one micron along both, i and j directions. The lifetimes of minority carriers as functions of doping were obtained from a public source[11]. The minority current carriers diffusion coefficients D_p (holes) and D_n (electrons) were calculated from Einstein's relationship using the appropriate mobilities listed in Table 3.

Table 1. The Inverter Layout Dimensions

OBJECT	DIMENSION (μm)
N^+ contact	40 x 60
P^+ S/D diffusions	10 x 160
N^+ S/D diffusions	10 x 160
P-well	60 x 400
N^+ contact/P^+ diffusion separation (edge to edge)	110
P^+ contact	7.5 x 160
P^+ contact/N^+ diffusion separation (edge to edge)	3
P^+ diffusion/p-well separation (edge to edge)	70
Substrate thickness	120
P-well depth	10
Diffusions depth	2

Figures 9 and 10 are three-dimensional maps of time-independent relative hole and electron concentrations inside the substrate and the P-well of the CMOS inverter when both parasitic transistors (lateral pnp and vertical npn) are in the active mode. The emitter P^+/substrate boundary nodes (26, 1-2), (26-28, 3) and (28, 1-2) were connected to an independent voltage supply given by $V_{i,j} = c_0\ P_0(x_i,y_j) = 1$ V with $P_0 x_i,y_j$ defined by (2.19) and c_0 being equivalent to $(P_0(x_i,y_j))^{-1}$ cm^3 V.

The existence of two depletion regions is recognized inside both, the substrate and the P-well, namely the P^+ drain/substrate and the N+/P-well boundaries associated with the output signal and the P-well/substrate boundary. The nodes at these regions ((33,1-2), (33-35,3), (35, 1-2) and (43,1-5), (43-55,6), (55,1-5)) were set as described in Sec. 2.2.3.

Table 2. Substrate grid dimensions

direction	nodes	nodes separation (μm)
j	1 to 3	1
	3 to 7	2
	7 to 11	5
	11 to 18	10
i	1 to 60	5

Table 3. Model input parameters

parameter	magnitude
μ_{en}[5]	1300 $cm^2\ V^{-1}\ s^{-1}$
μ_{hp}[5]	450 $cm^2\ V^{-1}\ s^{-1}$
μ_{ep}[5]	850 $cm^2\ V^{-1}\ s^{-1}$
μ_{hn}[5]	400 $cm^2\ V^{-1}\ s^{-1}$
τ_p[5]	8.0×10^{-6} s
τ_n[5]	2.5×10^{-6} s
v_s (SiO_2)[7]	100 $cm\ s^{-1}$
v_s (contact)[7]	1.0×10^6 $cm\ s^{-1}$

The surface nodes (1-4,1), (10-25,1), (29-33,1) and (56-60,1) are covered with oxide layer therefore the surface recombination velocity v_s was set to 200 $cm\ s^{-1}$ (see Table 3). The recombination velocity at these surfaces depends on the type of treatment they received during the fabrication process.

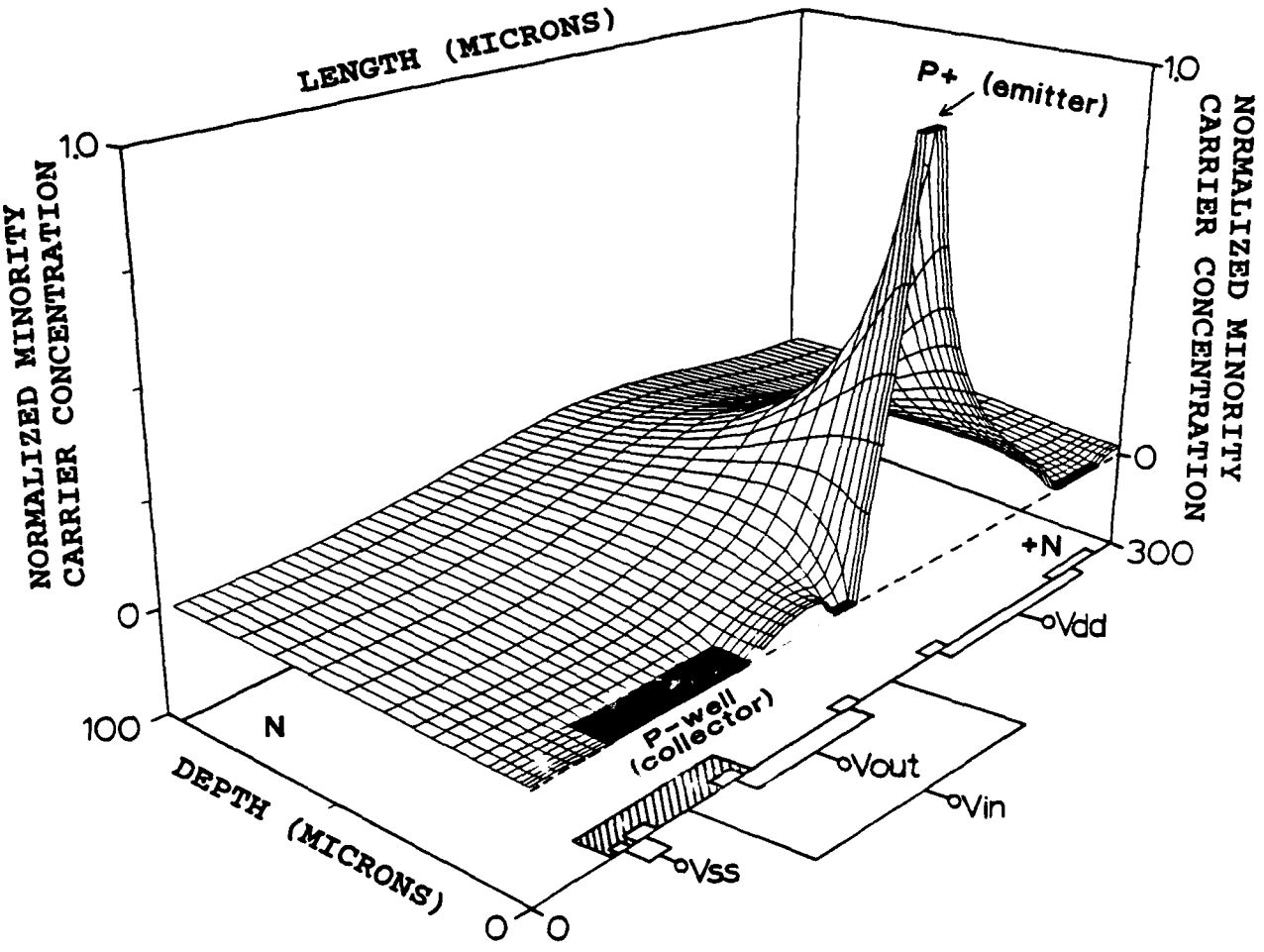

Figure 9: Time-independent normalized distribution of holes in the substrate of a CMOS inverter with active pnp transistor

For the electrolytical and chemical etching processes, the v_s values typically are several hundred cm s^{-1}[8]. The nodes located at the bottom surface of the substrate (1-60,18) had their surface recombination velocity set to the same value. The surface nodes (2-6,1), (18-37,1) and 49-59,1) of the P-well (figure 8) were also treated as surfaces under an oxide layer.

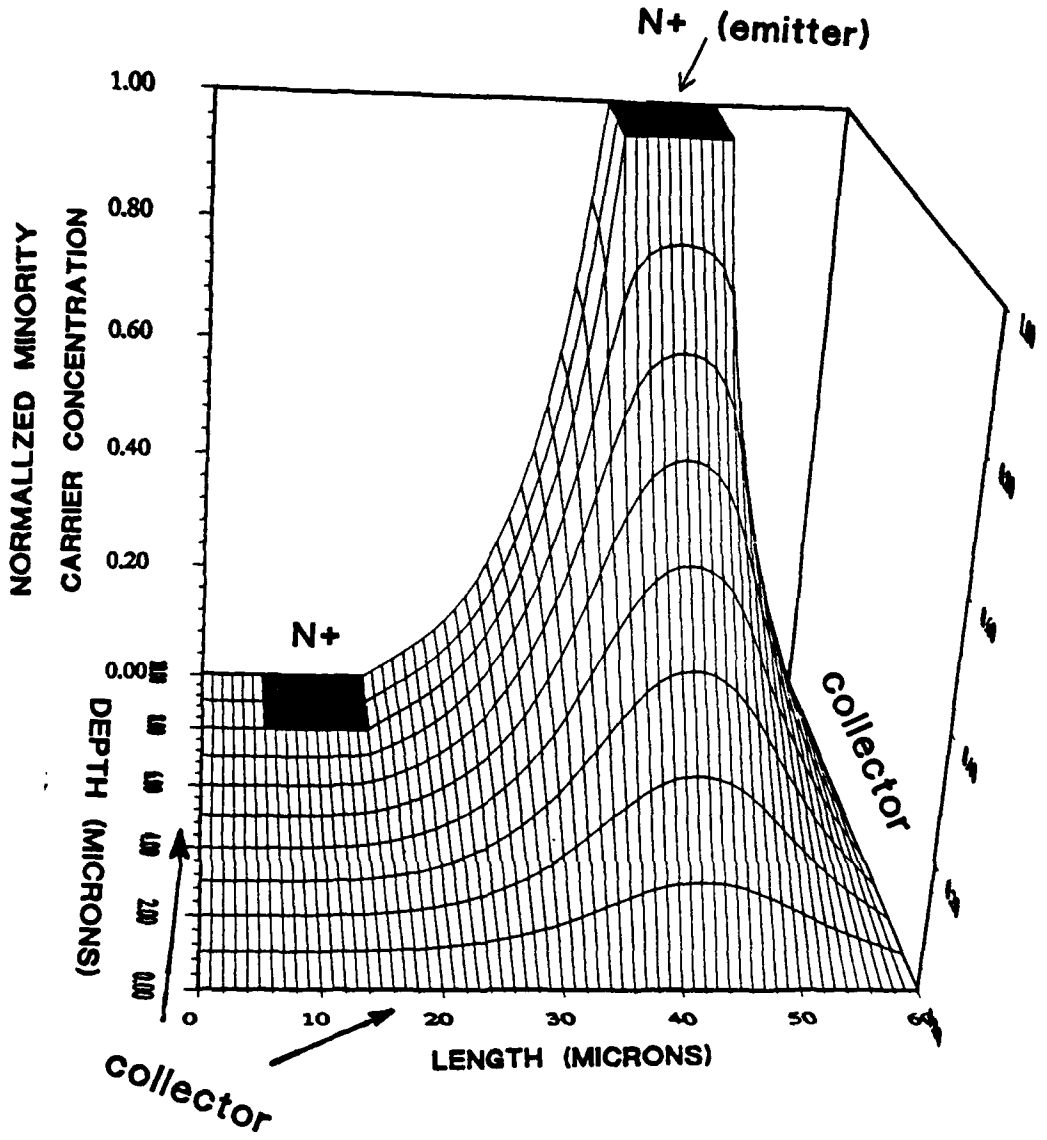

Figure 10: Time-independent normalized distribution of electrons inside the P-well of a CMOS inverter with active npn transistors

A rapid reduction in the density of minority current carriers at the vicinity of the emitters (figures 9 and 10) imply a presence of a strong diffusion current diverging into the semiconductor bulk ($I_{diff} = \nabla P(x_i, y_j)$. The bulk recombination process and the presence of depletion boundaries affect the current carrier concentration distribution. For example the concentration of current carriers located beneath the bottom

face of the emitter and the L.H.S of the emitter is mainly affected by the bulk recombination creating a density profile with an exponential decay. The carriers concentration between the emitter and the P-well, on the other hand, is strongly affected by the presence of depletion regions. Inside the P-well, being much smaller then the substrate, the bulk recombination effect becomes less important, and it is the depletion region surrounding the well that affects the distribution of the current carriers.

The close vicinity of the P+/substrate depletion boundary (figure 9) to the emitter causes an appreciable current to flow under the oxide-substrate interface (the surface between the P+ source and the P+ drain of the PMOS transistor). This will likely reduce the magnitude of the emitter diffusion current reaching the P-well/substrate (collector) boundary, which is known as the forward current ratio α. This important parameter, calculated from the results of the current transport study, determines the vulnerability of a particular device to latch-up. For the lateral pnp transistor it requires determining the ratio of the total current at the substrate / P-well depletion boundary with respect to the total current at P+ emitter / substrate boundary. Similarly, for the vertical npn transistor, the ratio sought is the one between the P-well / substrate and the N+ emitter/P-well boundaries. This was done by simply dividing the summed (over all nodes surrounding the collector) divided voltage differences at the collector by the equivalent sum obtained at the emitter.

Calculations indicate that only 12.6% of the total emitter current will ever reach the P-well. From this 57% will flow through near-side face of the P-well, 34% through the bottom face and 9% through the far-side face. The relatively low current gain of the parasitic lateral pnp transistor is attributed to the presence of an additional depletion region located between the emitter and the collector as well as the large distance between the two parts of device. In the case of the P-well, although the lifetime of the minority current is

about one third of the lifetime of holes in the substrate, the close proximity of the collector boundary gives this transistor a higher current gain. A total of 91% of the emitter current will reach the collector boundary. The majority of this diffusion current will be collected at the bottom face of the collector (91%), only ~9% will be collected at the near side boundary and virtually no emitter current will reach the far-side collector boundary.

4. The Lumped-Element Model

4.1 Latch-up Equivalent Circuit of a CMOS Inverter

The capacitive PN junctions formed at the boundary of diffusion wells are represented in the model as diodes. Small junctions such as the ones formed at the boundary of PMOS P+source/substrate well or the NMOS N+/P-well boundary (D1 and D5 in figure 11) are represented by a single diode. The P-well/substrate junction, on the other hand, due to its relatively larger extent (width = 60 μm), is modelled by three diodes shown as D2, D3, and D4 in figure 11. Multiple-diode representation of large well junctions takes into account the effect of the voltage drop in the substrate on the bias of the junction. Partially forward-biased junction of a large well can be then modelled by forward biasing the relevant diodes. This is done automatically during the execution of the program.

As shown in figure 11, the diodes in the model are not connected directly to the resistance grid but to voltage controlled voltage generators E_n. The voltage generators use the grid node voltages located in the vicinity of the diodes as a reference to maintain the voltage bias across the junction diodes. This connection decouples the diodes from the grid and allows treating the emitter currents that enter the substrate or the P-well as minority currents. This is done by

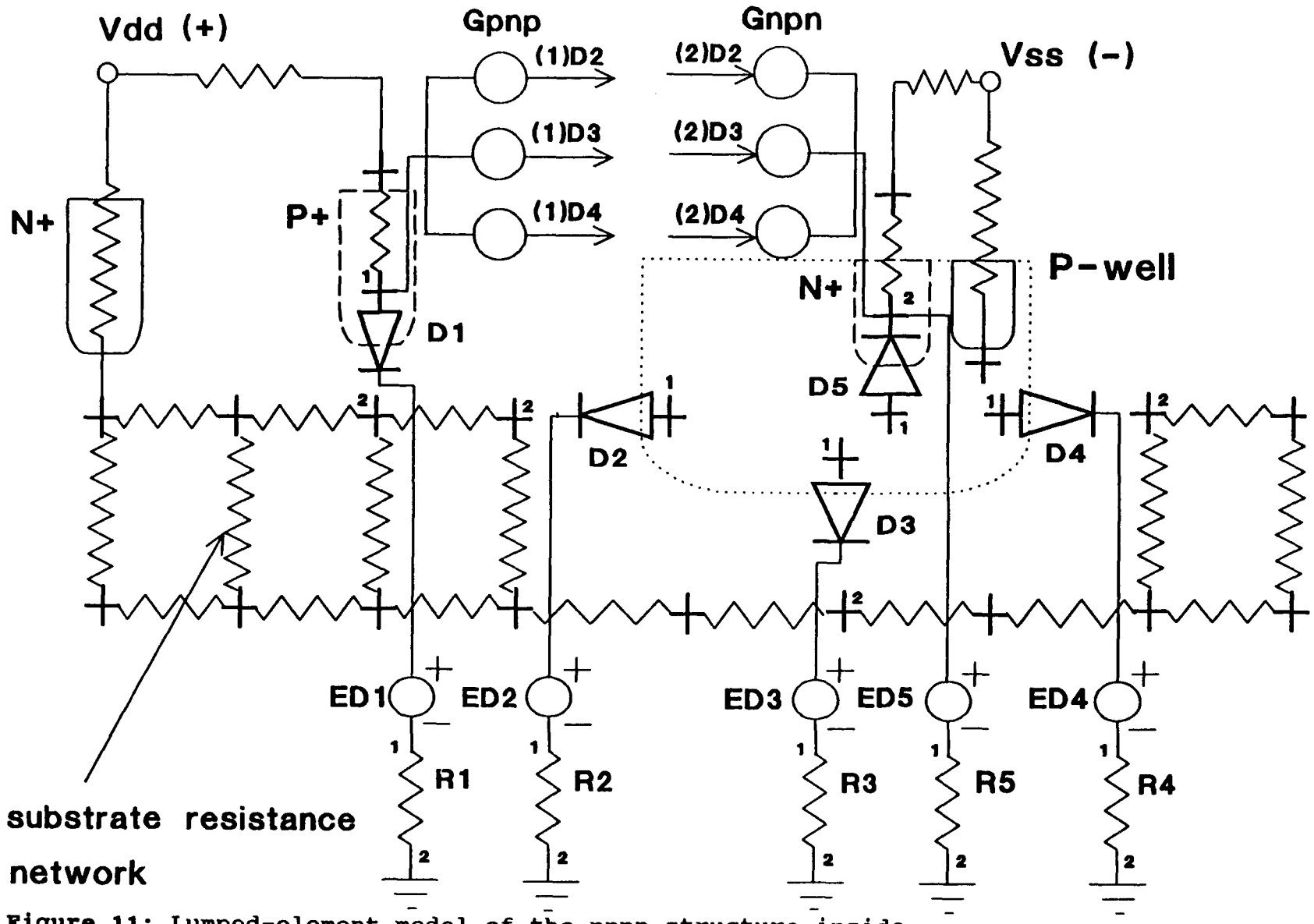

Figure 11: Lumped-element model of the pnpn structure inside a CMOS inverter.

adding a set of voltage controlled current generators, shown as $G_{pnp}D1D2$, $G_{pnp}D1D3$, $G_{pnp}D1D4$, $G_{npn}D5D2$, $G_{npn}D5D3$ and $G_{npn}D5D4$, thus forming a simple Ebers-Moll transport model[7]. The subscripts here refer to a transistor type and D_nD_m depicts the diodes representing the emitter and the collector sections respectively. The voltage controlled current generators use the difference in voltage drops across the resistors R_{nE} and R_{mC} to generate an output current which has a magnitude given by $I = G(V_n - V_m)$. The G parameter is a coefficient of a first degree polynomial with units of conductivity (Ω^{-1}).

The magnitudes of R_{nE} and R_{mC} has to be deduced in order to generate a model that would simulate the performance of a real device. This can be done with the aid of figure 12, which shows a simple Ebers-Moll transistor transport model (fig. 12a) and the equivalent circuit of a PNP transistor as connected in the model (fig. 12b). From Kirchhoff's current law, the collector current I_{C1} in the Ebers-Molls model is given by[7]

$$I_{C1} = I_r - \alpha_r I_r - \alpha_f I_f + \alpha_r I_r \qquad (4.1)$$

For the equivalent circuit in figure 11b, the collector current I_{C2} is

$$I_{C2} = I_r - \alpha_r I_r - G(V_n - V_m) \qquad (4.2)$$

with α_r and α_f as reverse and forward current transfer ratios and I_r and I_f as reverse and forward currents respectively. The voltages in (4.2) can be replaced by the current-resistance expressions (see panel b in figure 12) which after regrouping gives

$$I_{C2} = -GR_n(1-\alpha_f)I_f + GR_m(1-\alpha_r)I_r + (1-\alpha_r)I_r \qquad (4.3)$$

A term-by-term comparison with (4.1) with magnitude of G set to unity will result in

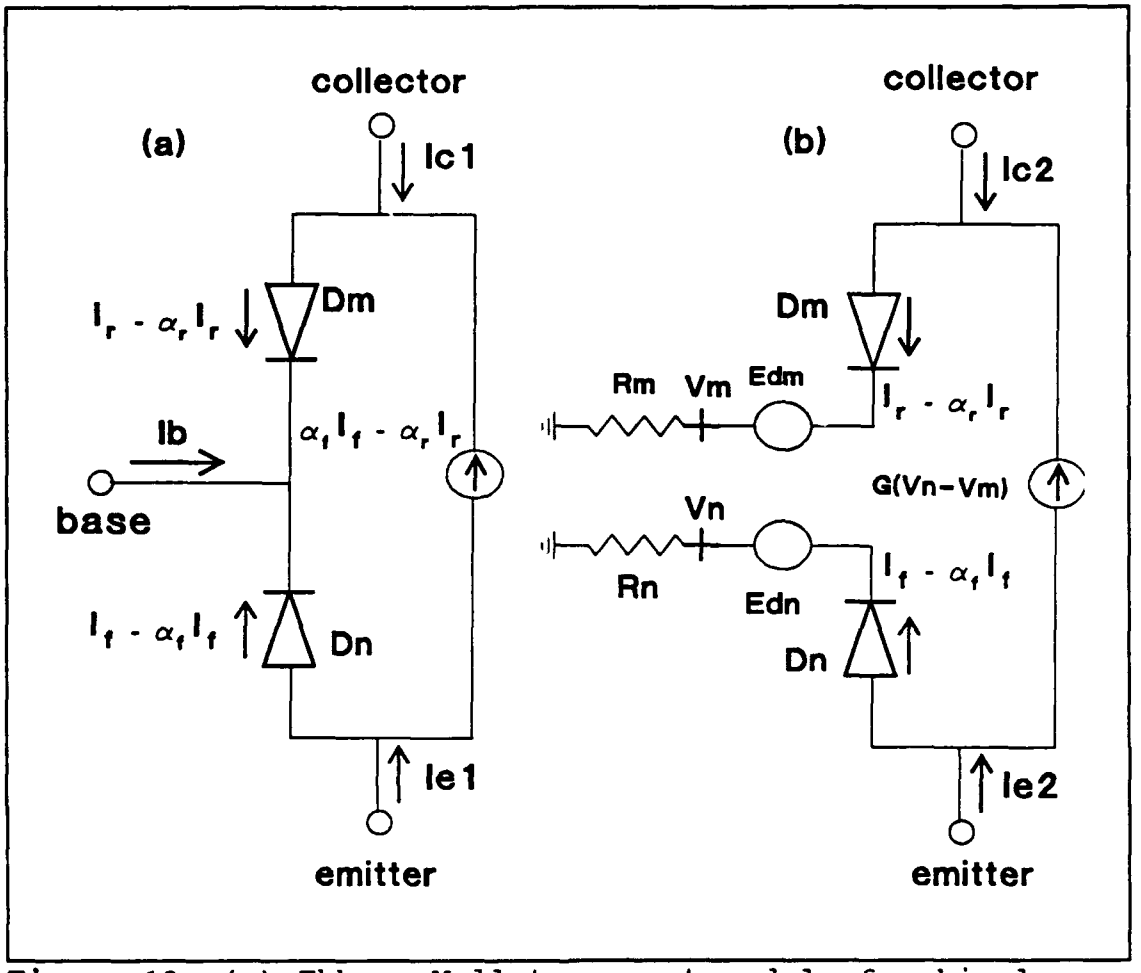

Figure 12: (a) Ebbers-Moll transport model of a bipolar pnp transistor
(b) Simulator transistor model

$$R_n(1-\alpha_f) = \alpha_f \;\therefore\; R_n = \frac{\alpha_f}{1-\alpha_f} = \beta_f \qquad (4.4)$$

and

$$R_m(1-\alpha_r) = \alpha_r \;\therefore\; R_m = \frac{\alpha_r}{1-\alpha_r} = \beta_r \qquad (4.5)$$

The results indicate that if the simulator circuit model is

to emulate the Ebers-Moll transistor model, the magnitudes of the resistors R_n and R_m must be numerically equivalent to forward (β_f) and reverse (β_r) gains of the transistor.

5. Model Application

5.1 Transient Response to Ionizing Radiation Dose Rate

The reference model circuit (see also Section 3) was subjected to simulated radiation dose rates of $\dot{\gamma} = 1.4 \times 10^9$ rad(Si) s^{-1} and $\dot{\gamma} = 1.8 \times 10^9$ rad(Si) s^{-1}. The latter rate referred to as the reference threshold dose rate, is the minum dose rate needed to latch-up the reference circuit model. In both trials the radiation pulse width was 1ns, with the rise/fall time of 0.1 ns and the pulse onset occurred at t = 0.5 ns.

The response of the model to the two dose rates is shown in figure 13. Several observations can be made with respect to the effect of ionizing radiation stimuli. Below the threshold dose rate, the voltages across the P+/substrate and N+/P-well junctions (figure 13) exhibit only a temporal change due to accumulation of the radiation-induced current carriers at the junctions followed by the junction discharge. Latch-up triggering occurs when both the primary photocurrent and the IR voltage drop due to the substrate current flow are able to forward bias the P+source / substrate and the N+drain / P-well junctions. For the reference model, this occurred at the dose rate of 1.8×10^9 rads/s. The constant potential across the junctions after the radiation pulse removal is then maintained by the substrate current.

Figure 14 shows the latch-up I-V characteristics of the reference model. The unstable operating voltage region is between 6 and 7 volts; the safe operating voltage for this device lies below 6 volts. Above this region ($V_{dd} > 7$ volts) the magnitude of the substrate current is relatively insensitive to the device operating voltage and during latch-up the holding current has a value of ~30 mA.

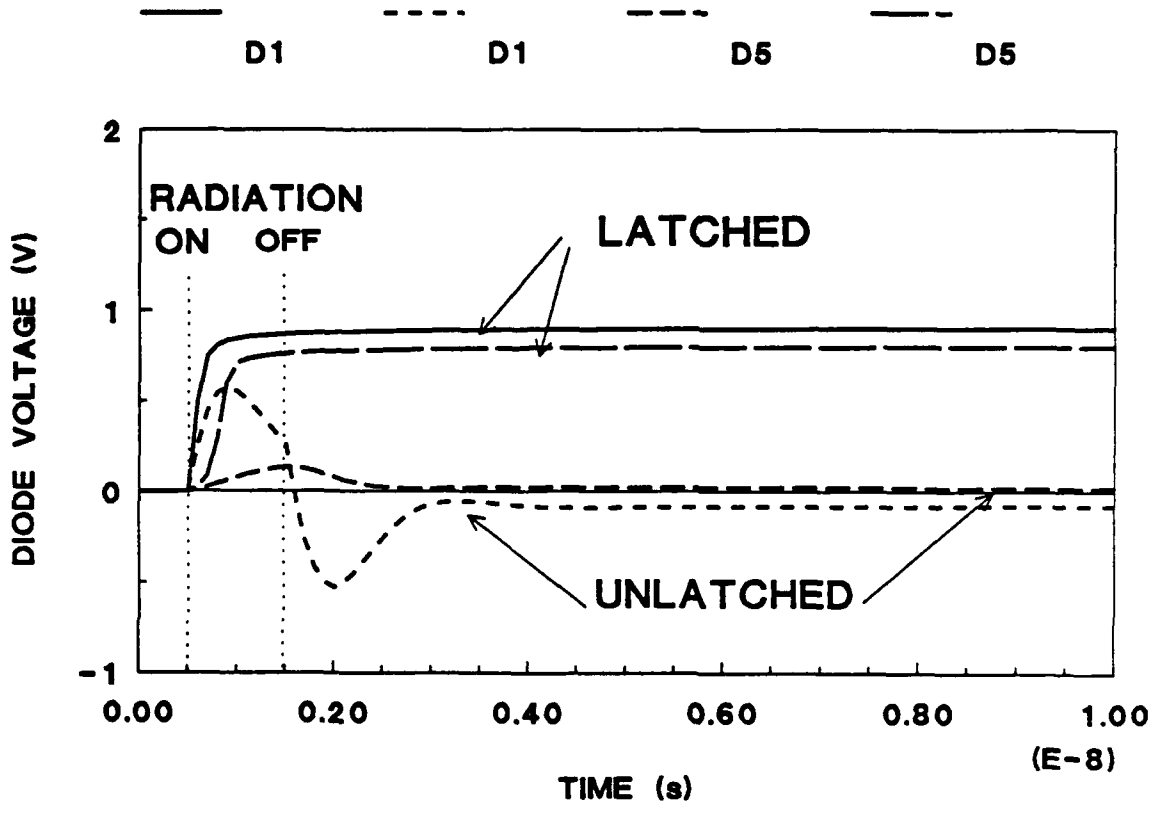

Figure 13: Voltage profiles across the emitter-base junctions at dose rates of 1.4×10^9 Rads(Si)/s and 1.8×10^9 Rads(Si)/s.

5.2. Effect of Layout and Circuit Features on Latch-up Susceptibility

The influence of layout and the substrate contact position on the latch-up sensitivity of a CMOS inverter is investigated here. The test structures of interest, referred to as Device #1 to Device #5 are presented in figure 15. Device #1 is the reference model with layout parameters given in Table 1. Device #2 has butted Vdd N+ substrate contact to P+ source reducing their effective distance from 110 μm to 30 μm. Device #3 has the same layout as Device #1 but has

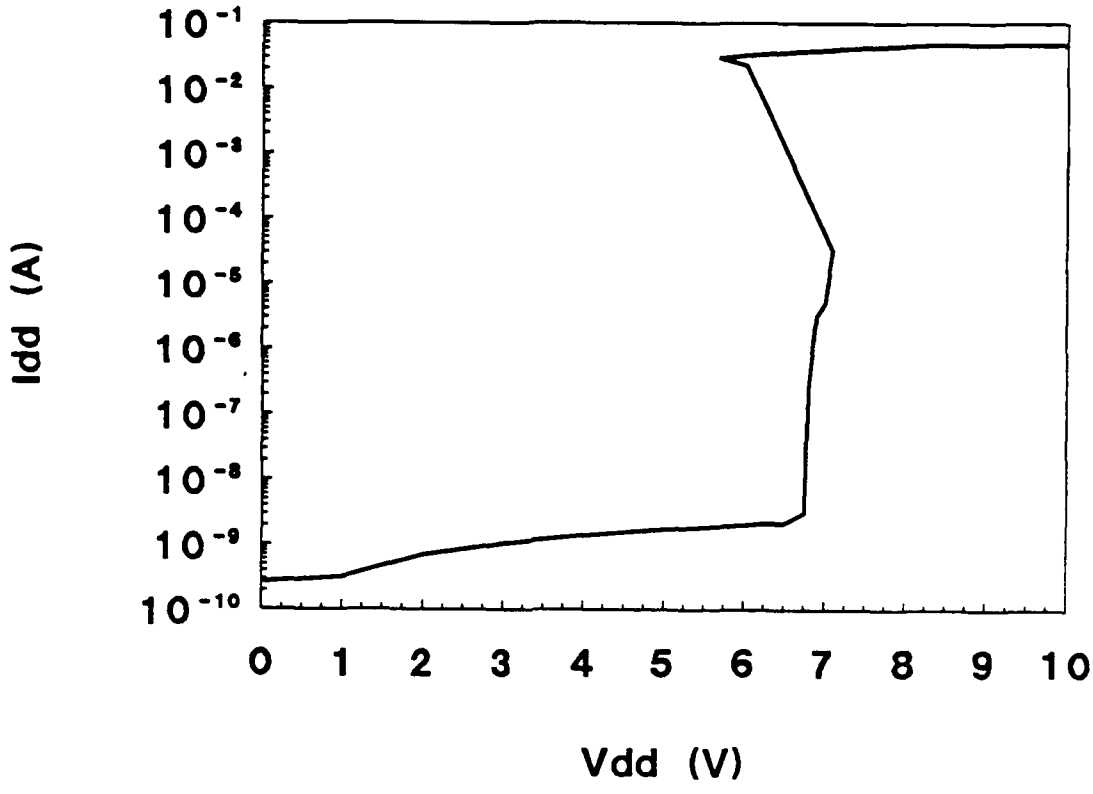

Figure 14: I-V characteristics of the reference inverter model

additional full V_{dd} contact at the back of the substrate. Test structures Device #4 and Device #5 have only half V_{dd} substrate contacts located opposite to N+ V_{dd} contact and opposite the P-well respectively.

Figure 16 shows that each test structure develops its own unique substrate current-flow pattern during the latch-up at the indicated threshold dose rates. The shading intensity relates to the current intensity (in mA) flowing into a particular semiconductor block. Figure 16a is the unlatched reference structure (Device #1) subjected to simulated dose rate of $\dot{\gamma} = 1.4 \times 10^9$ rads(Si) s^{-1} and figure 16b is the latched-up Device #1 subjected to the dose rate of $\dot{\gamma} = 1.8 \times 10^9$ rads (Si) s^{-1} (reference threshold dose rate).

Results show that the susceptibility of the circuit to latch-up decreases as the distance between the substrate N+

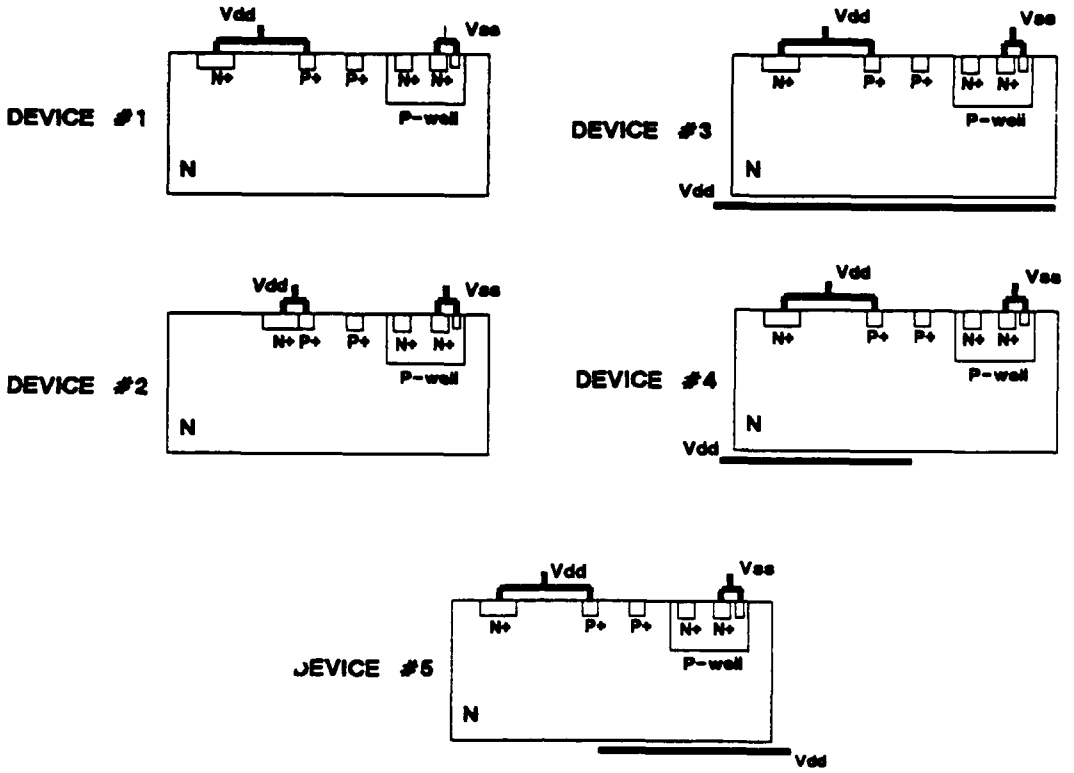

Figure 15: Inverter test structures utilized in the comparative study

V_{dd} contact and the P+ source of the PMOS transistor is reduced. For example the Device #2 (figure 16c) has a threshold dose rate of $\dot{\gamma} = 2.7 \times 10^9$ rads(Si) s^{-1} or about 50% higher then the reference threshold dose rate. This simulation result is in qualitative agreement with the measurements carried out earlier[3] on custom-made CMOS devices.

The test structures with a backside V_{dd} contact were found to exhibit the largest radiation-hardness. The relative position of the V_{dd} substrate contact with respect to the P-well determined their relative hardness. The threshold dose rate, for example, for the test structure with the full back contact (Device #3) is larger by a factor of about 900 than the reference threshold dose rate. The Device #4, where

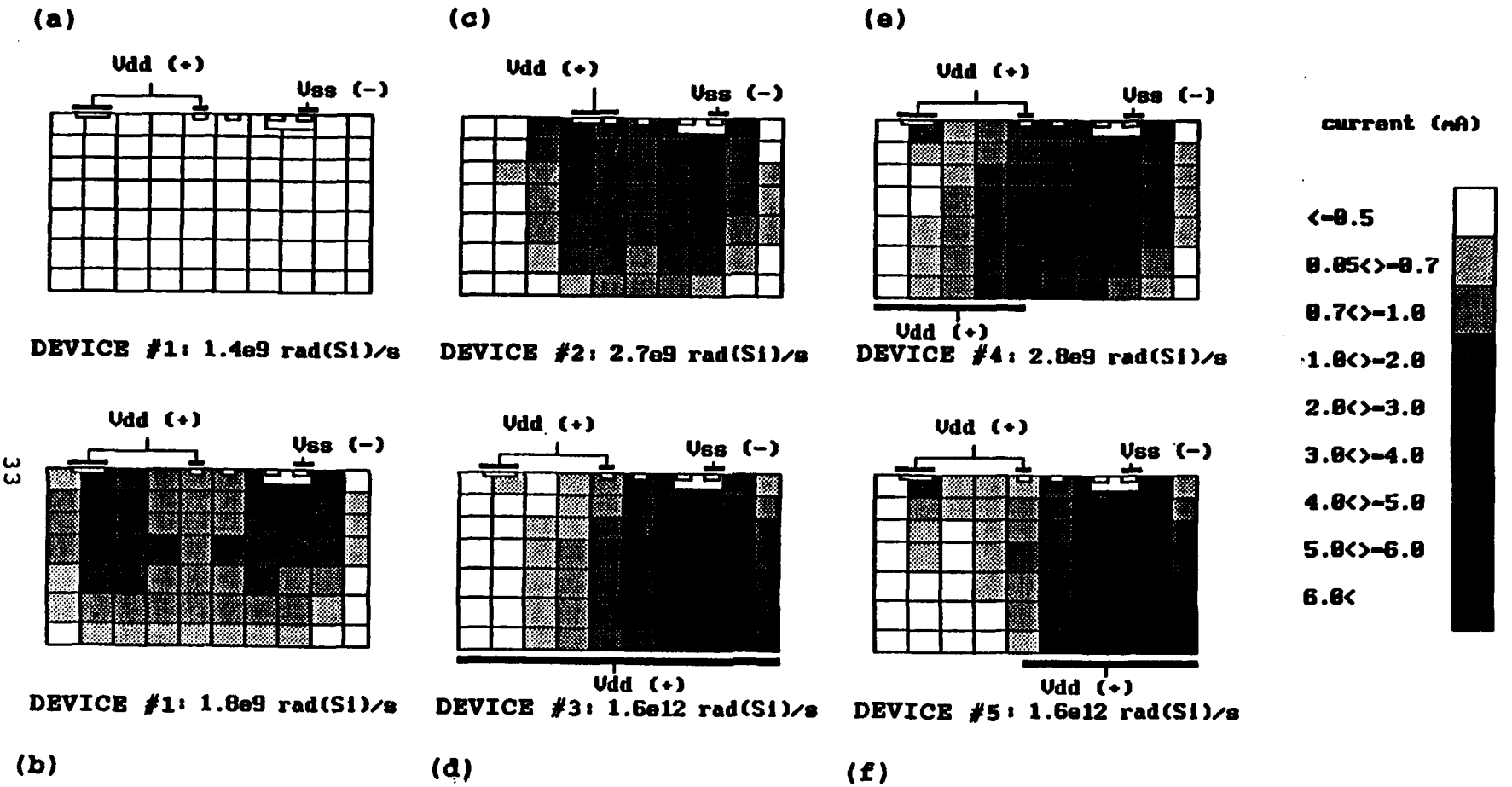

Figure 16: Substrate latch-up current distribution and threshold dose rates for the test structures in figure 15.

the back contact is situated just opposite to the N+ V_{dd} contact(figure 16d), was found to be only as rad-hard as Device #2. Placing the V_{dd} contact at the location just opposite the N+ substrate contact does increase the radiation hardness of the circuit, but only marginally.

Contribution of additional substrate contacts and their distribution to radiation hardness have been described in earlier studies[13]. The results that were obtained here are in agreement with such findings. Simulation such as this one, therefore, can be used as a pre-cursor to laser-induced latch-up experiments, where metallization has to be partially removed (due to a shadowing effect[14]) without changing appreciably the latch-up vulnerability of the circuit.

6. Discussion and Summary

A two-module discrete device simulator has been developed and applied to latch-up simulation studies using a simple CMOS inverter. It was shown that the diffusion module can be applied to calculate current gains of the parasitic transistors in CMOS structures. Implementation of bulk and surface recombination into the model also permits the investigation of the effects of doping profiles and surface treatment on the performance of a device. At present, the module can be applied to low-level injection case-studies of devices fabricated with extrinsic semiconductor materials. In such materials, the divergence of the electric field (caused by a local charge distribution) can be set to zero, simplifying the current equations and hence the device grid and calculations. This does not pose any serious limitation to practical applications since the majority of the devices are made of highly extrinsic semiconductor materials. For a broader range of applications, however, such as time-dependent simulations, SOS devices or SEU simulations, the diffusion module should be expanded to a two-carrier model, the inclusion of effects due to electric field(s) and time dependent effects.

The results obtained from the diffusion module of the model serve as input parameters for the lumped-element module. Due to the relatively low computing-time demand (less the 100 CPU seconds for the cases presented), utilization of the lumped-element module for latch-up studies in CMOS circuits appears to be well suited for application to complex CMOS structures. For asymmetrical structures, however, the latch-up path analysis necessitates 3-D analysis which requires considerably more computing power than for 2-D models of comparable resolution.

In conclusion, the general agreement between the model response to established radiation hardening techniques and the results carried out on real devices indicates the potential that exists in developing the model into a valuable CAD tool for device/circuit analysis.

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